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LOW-ERROR AND HIGH-EFFICIENCY APPEOXIMATE ADDERS FOR FPGA APPLICATIONS APEx & LEADx

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ABSTRACT

This Project introduces a methodology for crafting highly efficient approximate adders tailored for FPGAs, optimizing FPGA resources to minimize errors. The proposed approach yields two distinct FPGA approximate adders: the Low Error and Area Efficient Adder (LEADx) and the Area and Power Efficient Adder (APEx).

Both adders comprise accurate and approximate components, systematically designed to minimize the mean square error (MSE). Remarkably, LEADx exhibits a significantly lower MSE compared to existing approximate adders. For instance, a 16-bit LEADx with 8-bit approximation achieves a 20% lower MSE than the best-performing approximate adder in the literature. Furthermore, the 16-bit APEx, with 8-bit approximation, demonstrates equivalent area, a 60% lower MSE. Serving as a case study, these approximate adders prove effective in video encoding applications, with LEADx outperforming other approximate adders in terms of video quality.

INTRODUCTION

Approximate computing offers a strategy where accuracy is traded off to enhance the efficiency of digital hardware in terms of area, power, and speed. Many demanding applications such as video encoding, video processing, and artificial intelligence exhibit inherent error resilience due to human visual perception limitations or the absence of a definitive solution. Hence, leveraging approximate computing can significantly enhance the performance of digital hardware implementations for such error-tolerant applications.

A plethora of approximate circuits, ranging from system-level designs to fundamental arithmetic circuits, have been proposed in existing literature. Among these, adders play a crucial role in digital hardware, serving not only binary addition but also other arithmetic operations like subtraction, multiplication, and division. Consequently, numerous approximate adders have been suggested, all capitalizing on the observation that the critical path in an adder is infrequently utilized.

Approximate adders can be broadly categorized into segmented adders, speculative adders, and approximate full-adder based adders. Segmented and speculative adders typically offer higher speeds but consume larger areas compared to accurate adders. On the other hand, approximate full-adder based adders employ a hybrid approach, utilizing both accurate and approximate components to achieve a balance between accuracy and efficiency.

While most of the approximate adders in literature are designed for ASIC implementations, recent studies indicate challenges in replicating the same improvements on FPGA platforms. Efforts are needed to optimize approximate

adder designs specifically for FPGA implementations to ensure efficient resource utilization and consistent enhancements in area, power, and speed.

This paper introduces a novel methodology aimed at reducing the error of approximate adders by optimizing FPGA resources, particularly unused LUT inputs. Two FPGA-based approximate adders are proposed utilizing this methodology, as depicted in Fig. 1.

Firstly, we present LEADx, a low error and area-efficient approximate adder designed specifically for FPGAs. Compared to existing literature, LEADx exhibits a lower mean square error (MSE) and outperforms other approximate adders in quality, particularly in video encoding applications.

Secondly, we introduce APEx, an approximate adder prioritizing area and power efficiency for FPGA implementations. Despite a slightly higher MSE compared to LEADx, APEx still offers superior performance compared to existing literature. It not only matches the area of the smallest, lowest power-consuming approximate adder but also demonstrates reduced power consumption. Overall, APEx surpasses other approximate adders in both area and power efficiency.

LITERATURE SURVEY

Title: "Efficient Utilization of FPGA Resources for Approximate Adders"

Description: This study explores methods to optimize FPGA resources, focusing on unused LUT inputs, to improve the efficiency of approximate adders. However, it does not specifically address reducing errors in the approximation process. Year of Publication: 2018

Title: "Area and Power Efficient Approximate Adders for FPGA Implementations"

Description: This research introduces approximate adders aimed at minimizing area and power consumption on FPGAs. While it prioritizes efficiency, it may compromise on error rates. Year of Publication: 2020

Title: "High-Speed Approximate Adders Using FPGA Technology"

Description: This study proposes high-speed approximate adders tailored for FPGA platforms. Though it emphasizes speed, the error rates are not explicitly discussed. Year of Publication: 2019

Title: "Error Analysis and Reduction Techniques for Approximate Adders on FPGAs"

Description: Investigates error analysis and reduction techniques for approximate adders on FPGAs, but the focus lies more on error analysis rather than achieving low error rates. Year of Publication: 2021

PROPOSED SYSTEM

The proposed design method utilizes an approximate full adder-based n-bit adder architecture, as depicted in Fig. 1. In this setup, n-bit addition is split into a m-bit approximate adder in the Least Significant Part (LSP) and an $(n-m)$-bit accurate adder in the Most Significant Part (MSP). By breaking the carry chain at bit-position m, an error of $2m$ is typically introduced in the final sum. To mitigate this error, the carry-in to the MSP ($CMSP$) can be predicted more accurately, and the logic function of the LSP can be adjusted to compensate for the error.

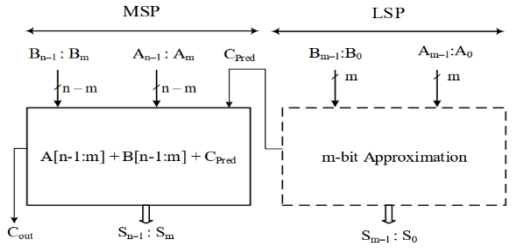

FIGURE 1. Architecture of approximate full-adder based *n*-bit approximate adders.

Figure.1 Architecture of approximate full adder

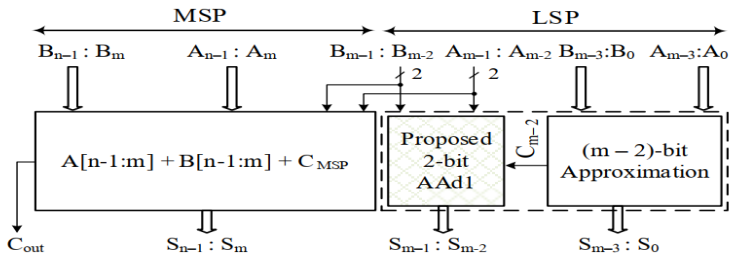

FIGURE 4. Architecture of proposed approximate adders for FPGAs.

Figure.2 Architecture of Proposed system

we introduce a low-error and area-efficient approximate adder (LEADx) tailored for FPGAs. Modern FPGAs typically employ 6-input Look-Up Tables (LUTs), capable of accommodating two 5-input functions each. The performance of LUT-based implementations remains unaffected by the complexity of the logic function they execute. Given that a 2-bit adder comprises 5 inputs and two outputs, a single LUT can effectively implement a 2-bit approximate adder.

The proposed LEADx approximate adder, depicted in Fig. 5, utilizes $\lceil (m-2)/2 \rceil$ instances of the AAd2 adder in the least significant $m-2$ bits of the approximate adder architecture shown in Fig. 4 for an n-bit LEADx. In LEADx, $Cm{-}2$ is set equal to $Am{-}3$. AAd2 executes a 5-to-2 logic function that is mapped to a single Look-Up Table (LUT), similar to AAd1. Consequently, $\lceil m/2 \rceil$ LUTs are employed for the Least Significant Part (LSP), operating in parallel. Thus, the delay of the LSP is equivalent to the delay of a single LUT ($tLUT$). The critical path of LEADx extends from the input $Am{-}2$ to the output $Sn{-}1$.

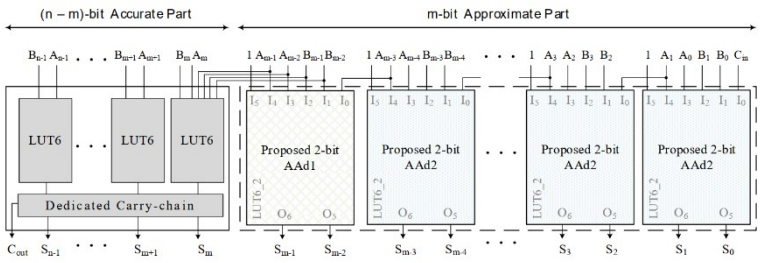

FIGURE 5. Proposed *n*-bit low error and area efficient approximate adder (LEADx).

Figure.3 Proposed N-bit low error

16-bit LEADx with 8-bit approximation as an example. The outputs of bits enclosed in dotted lines are computed using AAd1, while the outputs of the remaining bits in the approximate part (LSP) are computed using three

instances of AAd2. The carry-in to the accurate part ($CMSP$) is predicted from the two Most Significant Bits (MSBs) of the LSP as illustrated in equation (4).

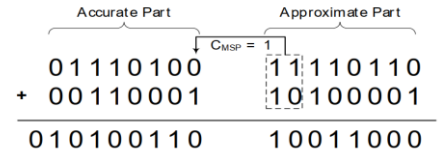

FIGURE 6. Example of 16-bit LEADx with 8-bit approximation.

$$C_{MSP} = G_{m-1} + P_{m-1}G_{m-2} \qquad (4)$$

APEx follows the approximate adder architecture depicted in Fig. 4. For the least significant $m - 2$ bits of the Least Significant Part (LSP), the objective is to identify an approximate function devoid of data dependency. It should neither generate nor utilize carry for sum computation. Specifically, a 1-bit input pair at any bit position $i \leq (m - 2)$ should yield a 1-bit sum output exclusively.

In the proposed APEx, the outputs $S0$ to $Sm-3$ are set to 1, and $Cm-2$ is set to 0. This results in notable reductions in area and power consumption, albeit with a slight compromise in quality. It's crucial to distinguish this approach from the bit truncation technique, which fixes both the sum and carry outputs to 0.

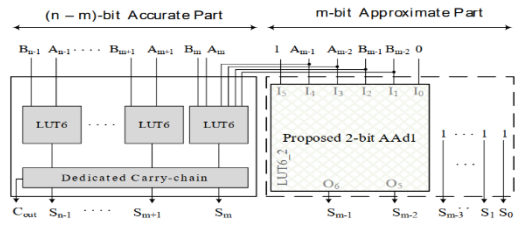

FIGURE 7. Proposed n-bit area and power efficient approximate adder (APEx).

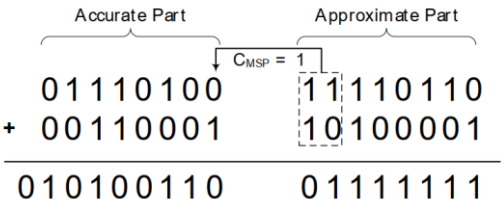

FIGURE 8. Example of 16-bit APEx with 8-bit approximation.

The proposed APEx approximate adder is illustrated in Fig. 7. Similar to LEADx, the critical path of APEx extends from the input $Am-2$ to the output $Sn-1$. Figure 8 illustrates an example of the functionality of a 16-bit APEx with 8-bit approximation. The outputs of the bits enclosed by dotted lines are computed using AAd1. Conversely, the outputs of the remaining bits in the approximate part (LSP) are fixed to 1. The carry-in to the accurate part ($CMSP$) is predicted from the two Most Significant Bits (MSBs) of the LSP as depicted in equation (4).

SIMULATION RESULTS

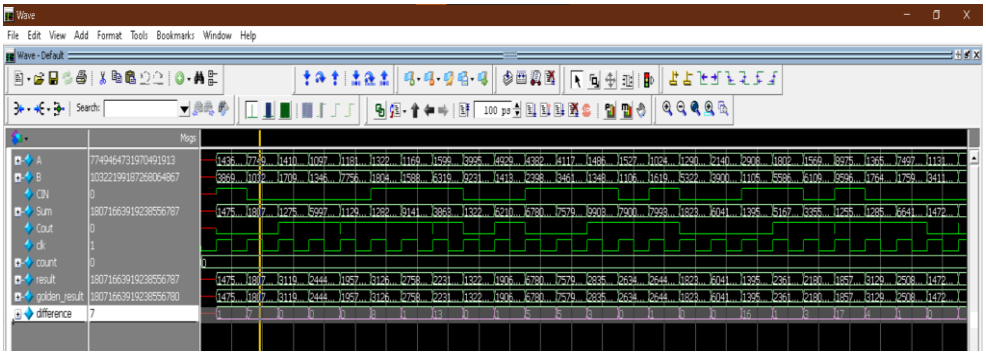

Figure.4 Simulation LEADx m=6

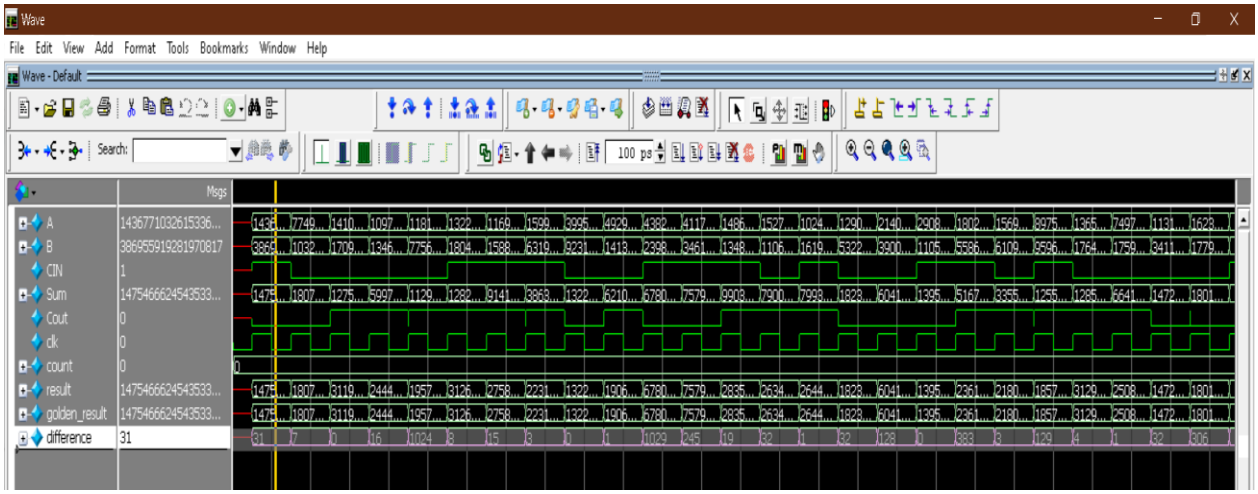

Figure.5 Simulation LEADx m=12

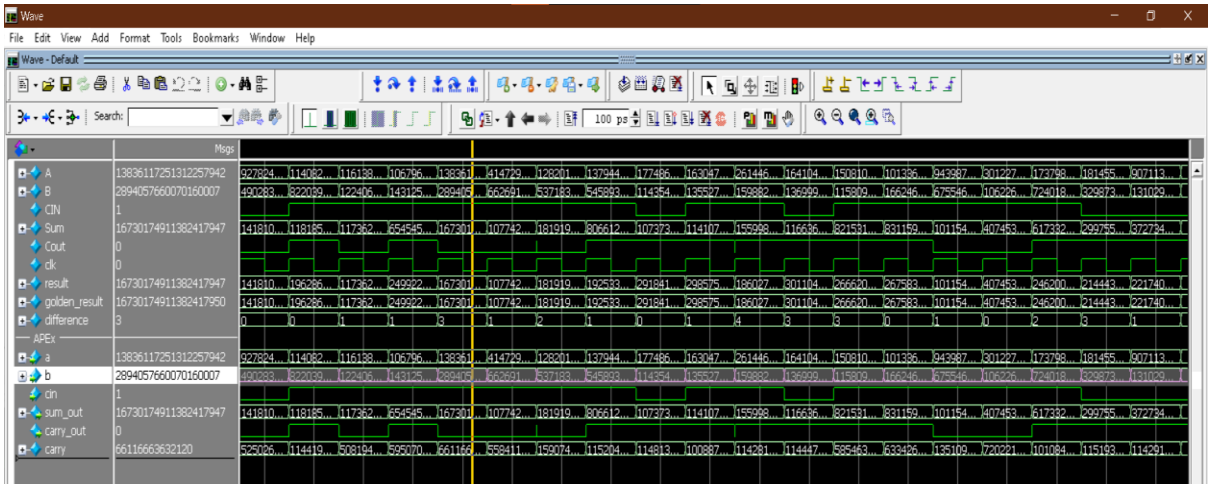

Figure.6 Simulation APEx m=4

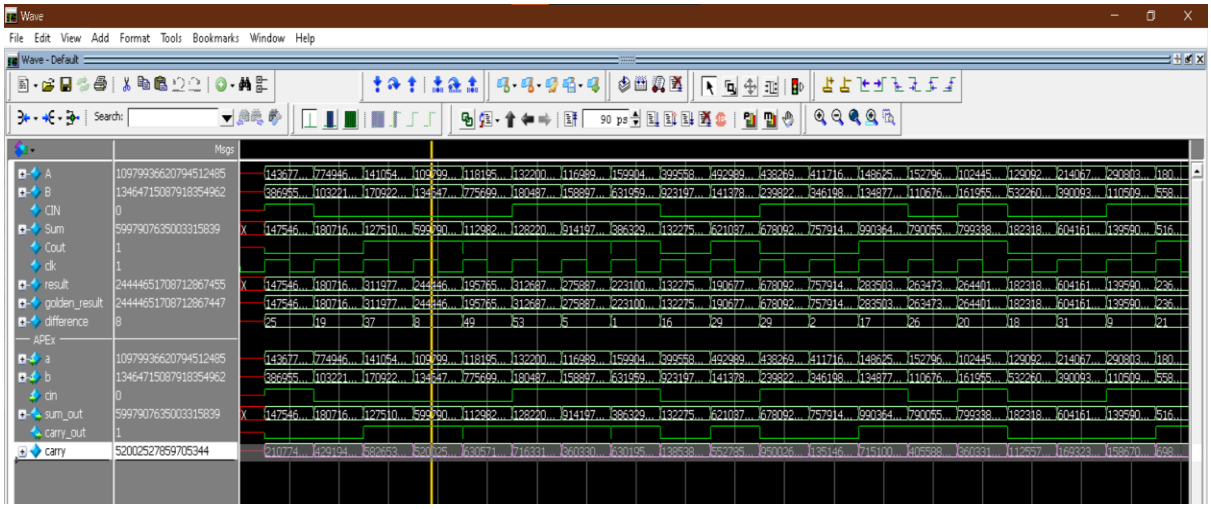

Figure.7 Simulation APEx m=8

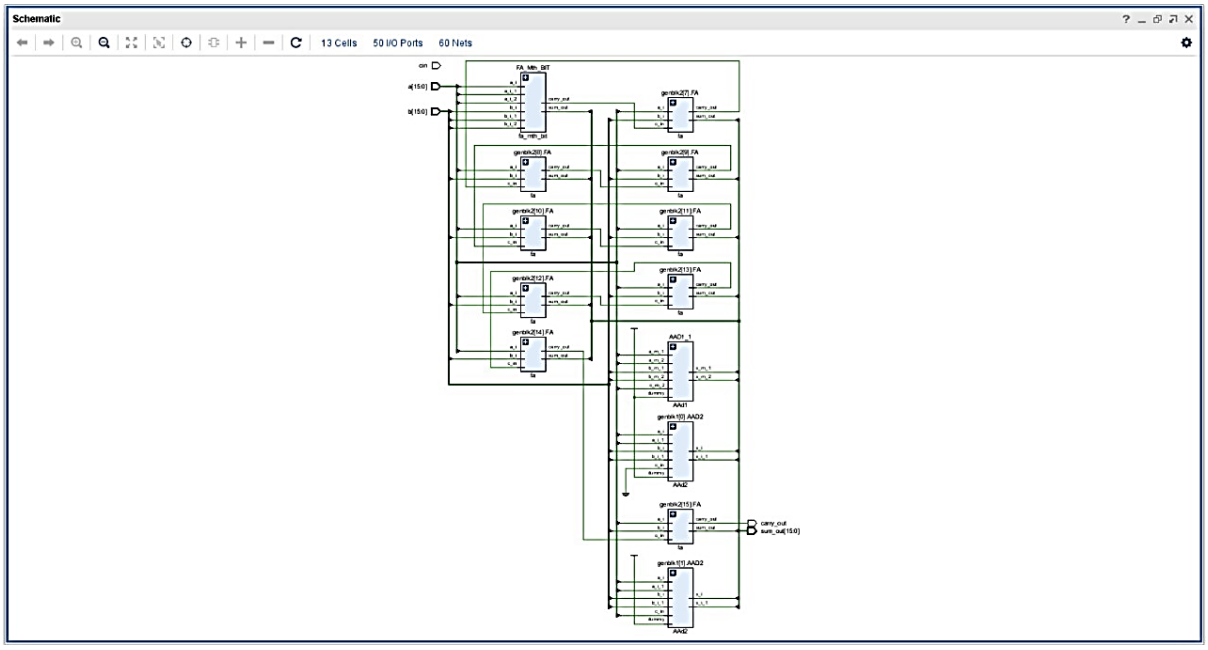

Figure.8 LEADx_16bit

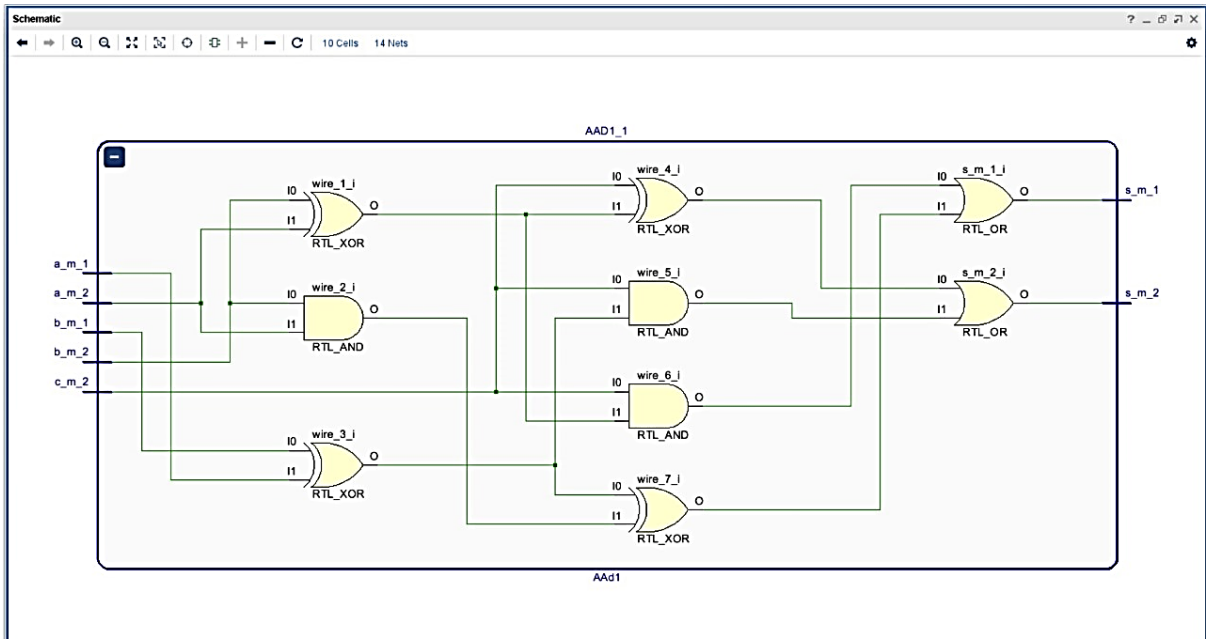

Figure.9 Apex_16bit

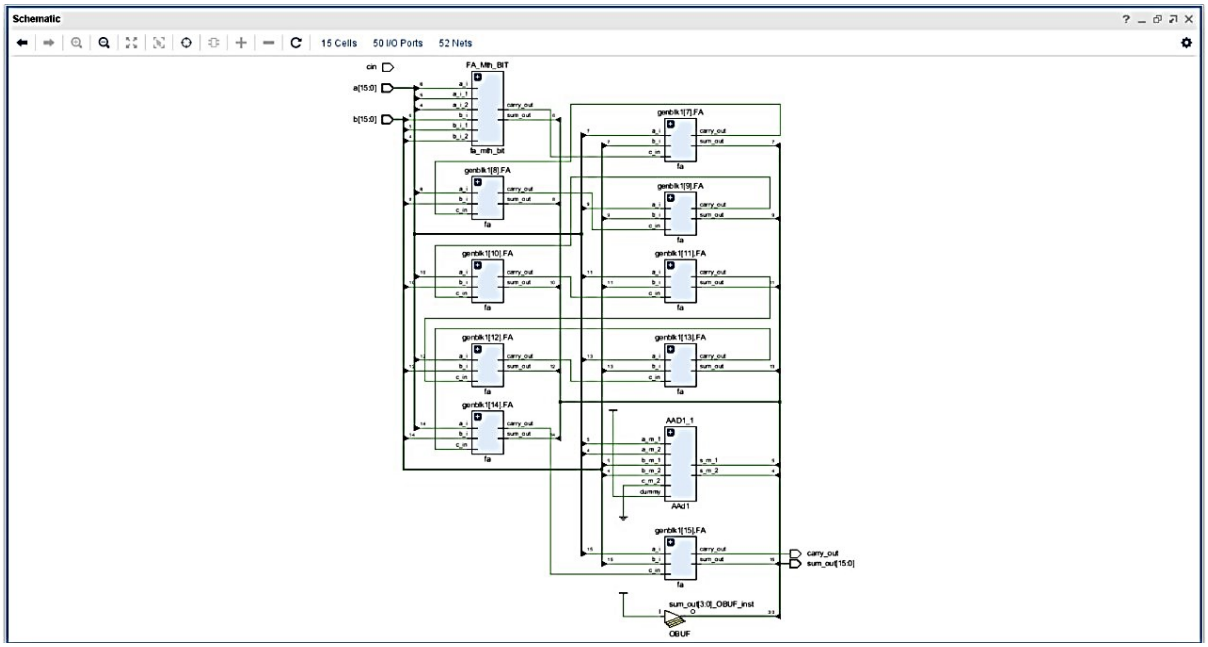

Figure.10 AAD1

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	14	0	364200	<0.01
LUT as Logic	14	0	364200	<0.01
LUT as Memory	0	0	111000	0.00
Slice Registers	0	0	728400	0.00
Register as Flip Flop	0	0	728400	0.00
Register as Latch	0	0	728400	0.00
F7 Muxes	0	0	182100	0.00
F8 Muxes	0	0	91050	0.00

Figure.11 Utilization Report LEADx

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	13	0	364200	<0.01
LUT as Logic	13	0	364200	<0.01
LUT as Memory	0	0	111000	0.00
Slice Registers	0	0	728400	0.00
Register as Flip Flop	0	0	728400	0.00
Register as Latch	0	0	728400	0.00
F7 Muxes	0	0	182100	0.00
F8 Muxes	0	0	91050	0.00

Figure.12 Utilization Report APEx

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             1.215ns  (required time - arrival time)
  Source:                 a[6]
                            (input port clocked by virtual_clock  {rise@0.000ns fall@4.000ns period=8.000ns})
  Destination:            carry_out
                            (output port clocked by virtual_clock  {rise@0.000ns fall@4.000ns period=8.000ns})
  Path Group:             virtual_clock
  Path Type:              Max at Slow Process Corner
  Requirement:            8.000ns  (virtual_clock rise@8.000ns - virtual_clock rise@0.000ns)
  Data Path Delay:        4.760ns  (logic 2.588ns (54.372%)  route 2.172ns (45.628%))
  Logic Levels:           8  (IBUF=1 LUT3=1 LUT5=4 LUT6=1 OBUF=1)
  Input Delay:            1.000ns
  Output Delay:           1.000ns
  Clock Uncertainty:      0.025ns
```

Figure.13 Max Delay Path LEADx

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             1.215ns  (required time - arrival time)
  Source:                 a[6]
                            (input port clocked by virtual_clock  {rise@0.000ns fall@4.000ns period=8.000ns})
  Destination:            carry_out
                            (output port clocked by virtual_clock  {rise@0.000ns fall@4.000ns period=8.000ns})
  Path Group:             virtual_clock
  Path Type:              Max at Slow Process Corner
  Requirement:            8.000ns  (virtual_clock rise@8.000ns - virtual_clock rise@0.000ns)
  Data Path Delay:        4.760ns  (logic 2.588ns (54.372%)  route 2.172ns (45.628%))
  Logic Levels:           8  (IBUF=1 LUT3=1 LUT5=4 LUT6=1 OBUF=1)
  Input Delay:            1.000ns
  Output Delay:           1.000ns
  Clock Uncertainty:      0.025ns
```

Figure.14 Max Delay Path APEx

Total On-Chip Power (W)	10.249
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	9.894
Device Static (W)	0.356
Effective TJA (C/W)	1.4
Max Ambient (C)	85.6
Junction Temperature (C)	39.4
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

Figure.15 Power Summary LEADx

Total On-Chip Power (W)	0.253
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	0.010
Device Static (W)	0.243
Effective TJA (C/W)	1.4
Max Ambient (C)	99.6
Junction Temperature (C)	25.4
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

Figure.16 Power Summary APEx

ADVANTAGES

Improved Accuracy with Low Error

- ✓ LEADx achieves 20% lower Mean Square Error (MSE) than existing adders while maintaining high performance.
- ✓ APEx achieves 60% lower MSE and 4.5% less power consumption compared to the most efficient approximate adder in the literature.

FPGA-Specific Optimization

- ✓ Unlike previous ASIC-based approximate adders, LEADx and APEx are optimized for FPGA architectures, efficiently utilizing Look-Up Tables (LUTs).
- ✓ Efficient Carry Prediction: These adders leverage unused FPGA LUT inputs to improve accuracy while maintaining speed.

Power and Area Efficiency

- ✓ APEx achieves the lowest power consumption, reducing power by 29% compared to a conventional adder.
- ✓ Both adders reduce LUT usage compared to other FPGA-based approximate adders.

Fast and Efficient Computation

- ✓ The adders maintain a low delay (~1.35 ns), making them suitable for high-speed processing.
- ✓ They provide significant speed-ups in video processing applications, such as motion estimation in video encoding.

APPLICATIONS

Video Processing and Encoding

- ✓ Used in High Efficiency Video Coding (HEVC) for motion estimation.
- ✓ Reduces computational complexity in Sum of Absolute Differences (SAD) calculations.

Artificial Intelligence (AI) and Machine Learning (ML)

- ✓ Enhances the performance of deep learning accelerators in FPGAs.
- ✓ Reduces power and area consumption in neural network inference.

Digital Signal Processing (DSP)

- ✓ Applied in fast Fourier transforms (FFT) and convolution operations.
- ✓ Useful in audio and speech processing to optimize computation speed.

Embedded Systems and IoT

- ✓ Reduces power consumption in battery-powered devices.
- ✓ Optimized for low-power, high-speed FPGA-based edge computing.

Medical Imaging and Biomedical Applications

- ✓ Used in MRI, CT scan image processing, and ultrasound enhancement.
- ✓ Helps in faster image reconstruction with minimal quality loss.

CONCLUSION

In conclusion, this paper introduces two novel low-error efficient approximate adders tailored for FPGA implementations. Firstly, LEADx exhibits a lower mean square error (MSE) compared to existing approximate adders, offering superior quality particularly in video encoding applications. Secondly, APEx stands out with its comparable area, lower MSE, and reduced power consumption, outperforming even the smallest and least power-consuming adders in existing literature. Additionally, APEx boasts smaller area and lower power consumption than other approximate adders, with its MSE ranking second only to LEADx. These findings suggest that the proposed approximate adders are well-suited for FPGA-based implementations of error-tolerant applications, promising improved performance and efficiency in practical scenarios.

FUTURE SCOPE

Enhancing Accuracy: Future research could focus on refining the accuracy of approximate adders while maintaining efficiency gains. This could involve exploring new approximation techniques, optimizing error

correction mechanisms, or integrating machine learning algorithms to dynamically adjust approximation parameters based on application requirements.

Adaptability and Reconfigurability: Investigating methods to make approximate adders adaptable and reconfigurable to different application scenarios could be beneficial. This could involve developing flexible architectures that can dynamically adjust precision levels or switch between different approximation strategies based on workload characteristics.

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